

WHAT IS CLAIMED IS:

1. A semiconductor wafer comprising:

at least one first sacrificial conductive line for supplying a first voltage to a plurality of dies fabricated on said wafer;

a plurality of integrated circuit dies fabricated on said wafer, each die comprising:

a first terminal coupled to the circuitry within said die for supplying a first voltage to said circuitry;

a second terminal for supplying a said first voltage to said first terminal;

a voltage interruption device provided between said first and second terminals for interrupting an electrical coupling between said first and second terminals; and

a first sacrificial terminal for receiving said first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal.

2. The wafer of claim 1 wherein each die further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal.

3. The wafer of claim 1 further comprising:

at least one second sacrificial conductive line for supplying a second voltage to said plurality of dies;

each die further comprising:

a third terminal coupled to the circuitry within said die for supplying a second voltage to said circuitry; and

a second sacrificial terminal for receiving said second voltage from said sacrificial second conductive line and supplying said second voltage to said third terminal.

4. The wafer of claim 3 wherein each die further comprises a second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal.

5. The wafer of claim 1 wherein the voltage interruption device is a fuse.

6. The wafer of claim 5 wherein said fuse is blown when a said die draws current in excess of a predetermined value.

7. The wafer of claim 3 wherein each die further comprises:

a passivation layer having respective openings to the first and second sacrificial terminals, said first and second sacrificial terminals respectively connecting with said first and second sacrificial conductive lines through said openings.

8. The wafer of claim 7 further comprising:

a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal; and

a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal.

9. A semiconductor die comprising:

a Vcc bonding pad coupled to the circuitry within said die for supplying a first voltage to said circuitry;

a secondary Vcc pad;

a fuse interconnected between the standard Vcc bonding pad and the secondary Vcc pad, said secondary Vcc pad supplying said first voltage through said fuse to the Vcc bonding pad, said fuse adapted for interrupting electrical coupling between the secondary and Vcc bonding pads when the die draws current in excess of said fuse breakdown current;

a sacrificial Vcc pad for receiving a first voltage; and

a sacrificial metal bus interconnected between the sacrificial Vcc pad and secondary Vcc pad for receiving a first voltage from the sacrificial Vcc pad and supplying said first voltage to the secondary Vcc pad.

10. The semiconductor wafer of claim 9 further comprising:

a Vss bonding pad coupled to the circuitry within said die for supplying a second voltage to said circuitry;

a sacrificial Vss pad for supplying the second voltage to the standard Vss pad; and

a sacrificial metal bus which connects the sacrificial Vss pad and the standard Vss bonding pad.

11. The semiconductor die of claim 10 further comprising:

a passivation layer which is provided with respective openings to the sacrificial Vcc and Vss pads; and

Vcc and Vss sacrificial conductive busses formed over said passivation layer, said Vcc sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vcc sacrificial pad and said Vss sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vss sacrificial pad.

12. A method of fabricating an integrated circuit die comprising:

forming a first terminal on said die which is coupled to circuitry within said die, said first terminal being adapted to supply a first voltage to said circuitry;

forming a second terminal adapted to supply said first voltage to said first terminal;

forming a voltage interruption device between said first and second terminals which is adapted to interrupt an electrical coupling between first and second terminals when predetermined operations of said circuitry occur; and

forming a first sacrificial terminal for receiving a first voltage and supplying said first voltage to said second terminal.

13. A method of claim 12 further comprising forming a first on-die sacrificial conductive line coupled between the second terminal and the first sacrificial terminal.

14. A method of claim 13 further comprising

forming a third terminal on said die which is coupled to circuitry within said die said third terminal being adapted to supply a second voltage to said circuitry; and

forming a second sacrificial terminal on said die for receiving a second voltage and supplying the second voltage to the third terminal.

15. A method of claim 14 further comprising forming a second sacrificial on-die conductive line coupled between the third terminal and second sacrificial terminal.

16. A method of claim 15 further comprising

forming a passivation layer over said die;

forming openings through the passivation layer exposing first and second sacrificial terminals on each die, said first and second sacrificial terminals supplying operating voltage to a respective die; and

forming a sacrificial metal layer over the passivation layer to provide a first conductive line connected to said first sacrificial terminal and a second conductive line connected to said second sacrificial terminal, the respective lines connecting to first and second sacrificial terminals through corresponding openings in the passivation layer.

17. A method of processing a semiconductor wafer containing at least one die comprising:

supplying a first voltage to a first sacrificial conductive line and a second voltage to a second sacrificial conductive line, said sacrificial conductive lines being provided on said wafer and connected respectively to a first and second sacrificial terminal said at least one die;

testing at least one die while said first and second voltage is applied;

blowing a current interruption device provided on said at least one die if the die draws current in excess of a predetermined value;

removing said first and second sacrificial conductive lines and the first and second sacrificial voltage terminals;

exposing on-die first and second terminals on said at least one die, said first and second terminals interconnected by said current interruption device; and testing the status of said current interruption device through said exposed first and second terminals.

18. A method of fabricating a die, said method comprising:

forming conductive structure on said die comprising:

- a Vcc bonding pad connected to die circuitry for receiving a first voltage;
- a secondary Vcc pad;
- a fuse interconnected between the Vcc bonding pad and the secondary Vcc pad;
- a sacrificial Vcc pad;
- a metal bus interconnecting the sacrificial Vcc pad and secondary Vcc pad;
- a Vss bonding pad connected to die circuitry for receiving another voltage;
- a sacrificial Vss pad; and
- a metal bus interconnecting the sacrificial Vss pad and the Vss pad.

19. The method of claim 18 further comprising:

- forming a passivation layer on the die;
- forming contact openings through passivation layer exposing the sacrificial Vcc and Vss pads on each die; and
- forming a Vcc and Vss sacrificial metal conductor over the passivation layer and into the openings respectively connecting with the Vcc and Vss sacrificial pads.

20. The method of claim 19 further comprising testing said fabricated die, said testing comprising:

applying Vcc and Vss voltage to said Vcc and Vss sacrificial metal conductors; and

blowing said fuse of said die which draws current in excess of a predetermined value.

21. The method as in claim 20 further comprising exposing said Vcc bonding pad and secondary Vcc pad and checking for fuse continuity between said pads;

22. The method as in claim 19 further comprising:

applying Vcc and Vss voltage to said Vcc and Vss sacrificial metal conductors; and

testing said die while said Vcc and Vss voltage is applied.

23. The method of claim 22 further comprising:

removing the sacrificial Vcc and Vss conductors;

removing the sacrificial Vcc and Vss pads; and

exposing the Vcc bonding pad, secondary Vcc pad and Vss bonding pads on each die.

24. The method as in claim 23 further comprising testing the continuity of said fuse using said exposed Vcc bonding pad and secondary Vcc pad.